**19EC2102 – FUNDAMENTALS OF DIGITAL CIRCUITS**

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| **Course category:** | Program core | **Credits:** | 3 |
| **Course Type:** | Theory | **Lecture - Tutorial - Practical:** | 3 - 0– 0 |
| **Prerequisite:** | Number systems ,Semiconductor device operations, basic Arithmetic operations | **Sessional Evaluation :****External Evaluation:****Total Marks:** | 4060100 |

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| **Course****Objectives** | Students undergoing this course are expected to understand: |
| 1. Introduce basic postulates of Boolean algebra and shows the correlation between Boolean expressions.
2. Introduce the methods for simplifying Boolean expressions.
3. Outline the formal procedures for the analysis and design of combinational circuits
4. Illustrate the concept of synchronous and asynchronous sequential circuits
5. Introduce the concept of various counters and Registers
6. Introduce the concept of memories and Memory expansion
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| **Course Outcomes** | Upon successful completion of the course, the students will be able to: |
| CO1 | Understand the fundamental concepts and techniques used in digital electronics and examine the structure of various number systems and its application in digital design |
| CO2 | Identify basic requirements for a design application and propose a cost effective solution  |
| CO3 | Understand, analyze and design various combinational circuits |
| CO4 | Understand, analyze and design various sequential circuits.  |
| CO5 | Identify and prevent various hazards and timing problems in a digital design. |
| CO6 | Understand the memories |
| **Course****Content****Course****Content** | **UNIT – I****NUMBER SYSTEMS AND CODES:** Number systems, Signed binary numbers, Base conversions, Binary arithmetic, Complements, Binary codes–(BCD, Excess-3, Grey, ASCII).**BOOLEAN ALGEBRA AND LOGIC GATES**: Theorems of Boolean algebra, De-Morgan’s theorem, Realization of logic gates using Universal gates.**UNIT – II****MINIMIZATION OF DIGITAL CIRCUITS:** Standard forms of logical functions, Min-term and max-term specifications, Simplification by K-maps, incompletely specified functions, Realization of logic functions using gates.**UNIT -III****COMBINATIONAL LOGIC CIRCUITS:** Design procedure, Binary adder, Sub-tractor, Decimal adder, Magnitude comparator, Decoders, Encoders, Multiplexers and De-multiplexers.**UNIT – IV****SEQUENTIAL CIRCUITS:** Sequential circuits, Storage Elements: (Latches & Flip-flops), Master-Slave Flip-flop, Race around condition, Flip-flop conversions, Timing and triggering considerations, State diagrams, state tables, reduction of state tables and state assignment, design procedures.**UNIT – V****REGISTERS AND COUNTERS:** Registers, Shift registers, Ripple counters, Synchronous counters, Ring and Johnson counters.**UNIT-VI****MEMORY AND PROGRAMMABLE DEVICES:** Random-Access Memory, Memory Decoding, Read-only Memory, Programmable Logic Array, Programmable Array Logic, Sequential programmable devices. |
| **Text Books and Reference Books** | **TEXT BOOKS:**1. Digital design by Morris Mano, Pearson Education Asia, 5th Ed., 2012
2. Fundamentals of logic design by Roth & Charles, 6th Edition, West Publishing Company, 2009.

**REFERENCES:**1. Fundamentals of logic circuits by A. Anand Kumar, PHI Learing, 2016
2. Jon M, Yarbrough, “Digital logic — applications and design”, Thomson-Brooks India edition
3. Fundamental of Digital Design By M. Senthil Sivakumar, S.Chand publications, 2014.
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| **E-Resources** | 1. http://nptel.ac.in/cources
2. https:// iete-elan.ac.in
3. <https://freevideolectures.com/university/iitm>
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| Contribution of Course Outcomes towards achievement of Program Outcomes  |
|  | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
| CO1 |  3 | 3 | 2 | 2 | 2 | - | - | - | - | - | - | 2 | 3 | 3 |
| CO2 | 3 | 3 | 2 | 2 | 2 | - | 2 | - | - | - | - | 2 | 3 | 3 |
| CO3 | 3 | 3 | 3 |  2 |  2 |  - |  - |  - |  - |  - |  2 |  2 |  3 |  3  |
| CO4 | 3 | 3 | 2 | 2 | 2 | - | - | - | - | 1 | 2 | 2 | 3 | 3 |
| CO5 | 3 | 3 | 2 | 2 | 2 | - | - | 2 | - | - | - | 2 | 3 | 3 |
| CO6 | 3 | 3 | 2 | 2 | 2 | - | - | - | - | - | - | 2 | 3 | 3 |